

Fig. 1

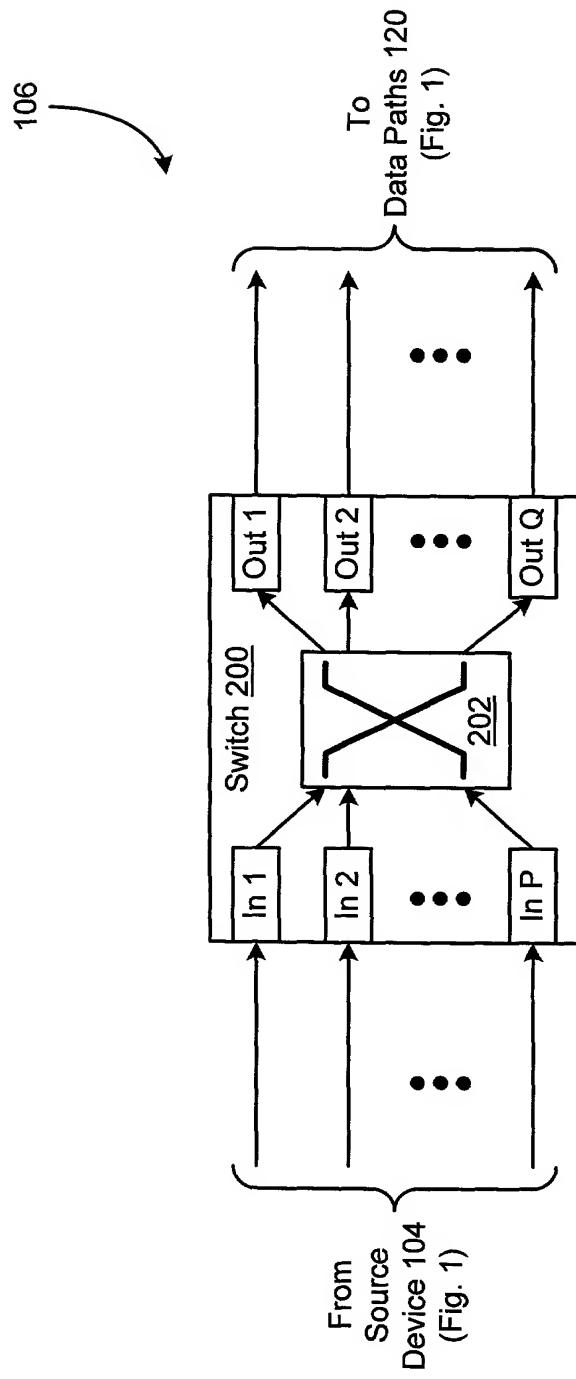


Fig. 2

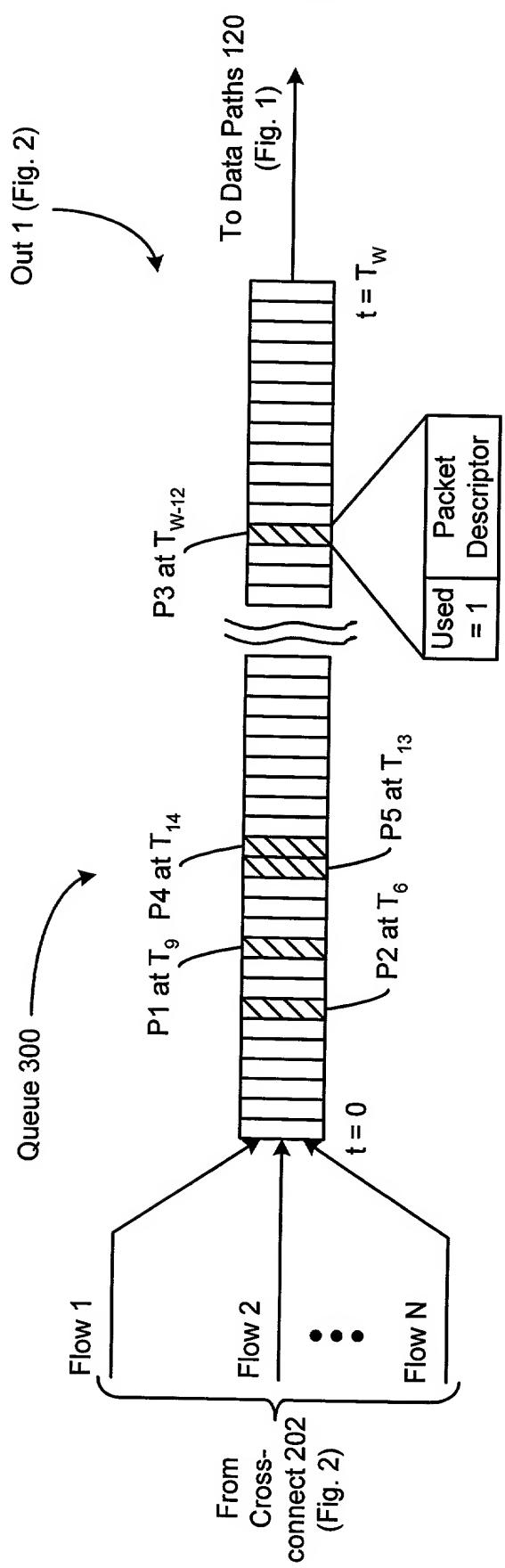


Fig. 3

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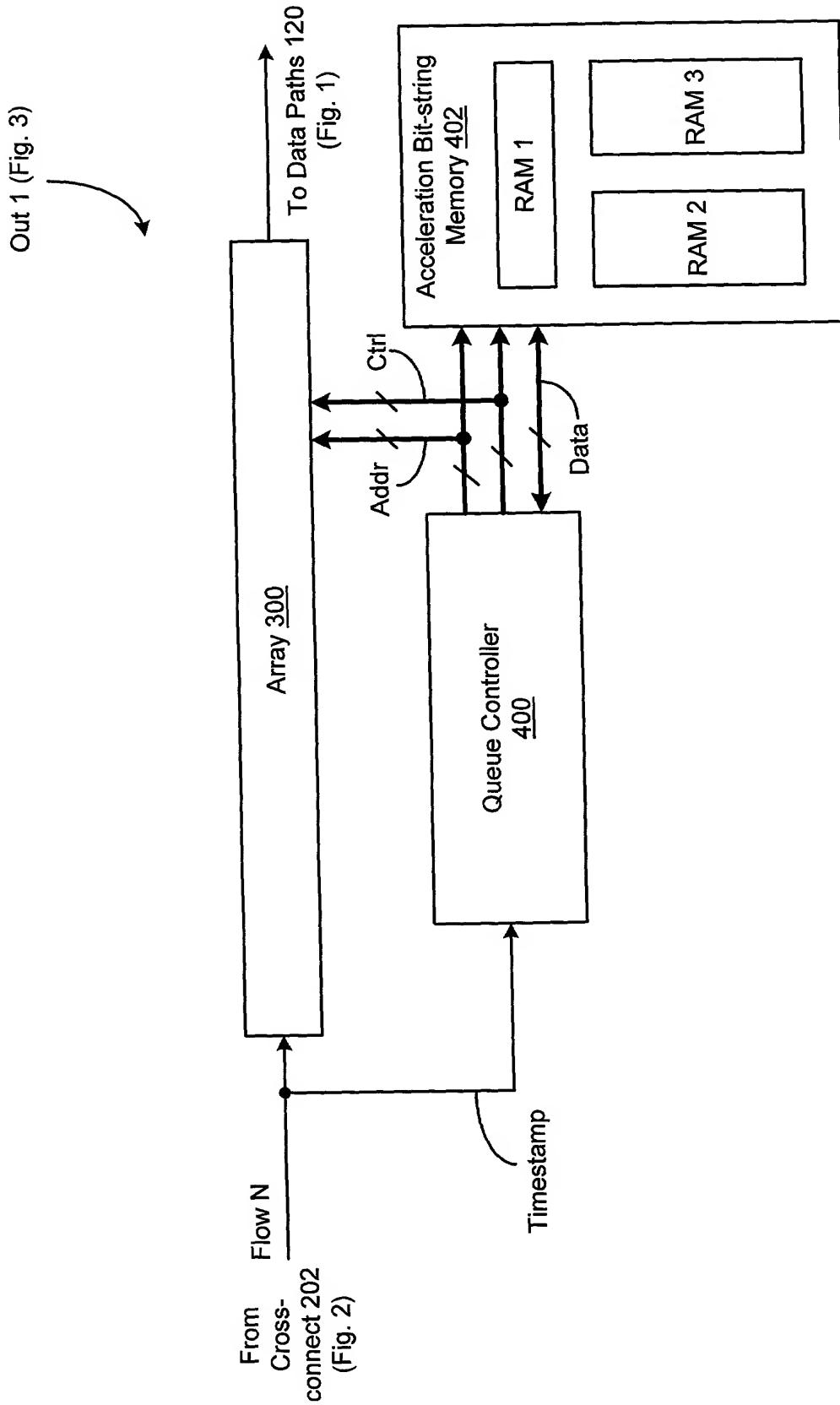


Fig. 4

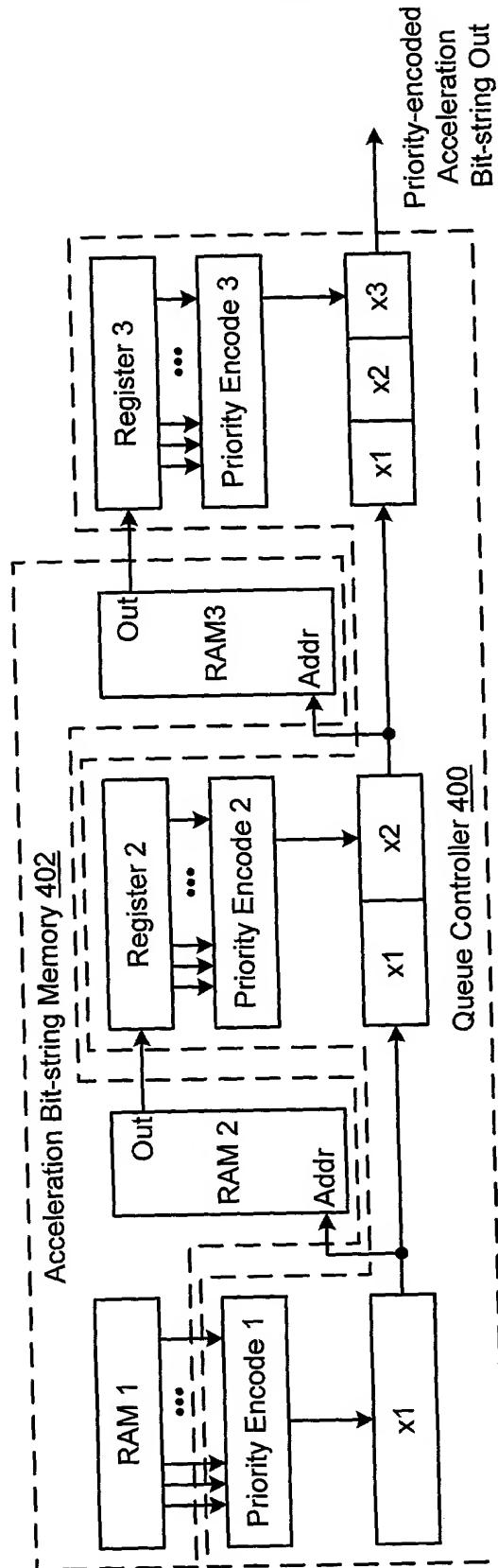


Fig. 5

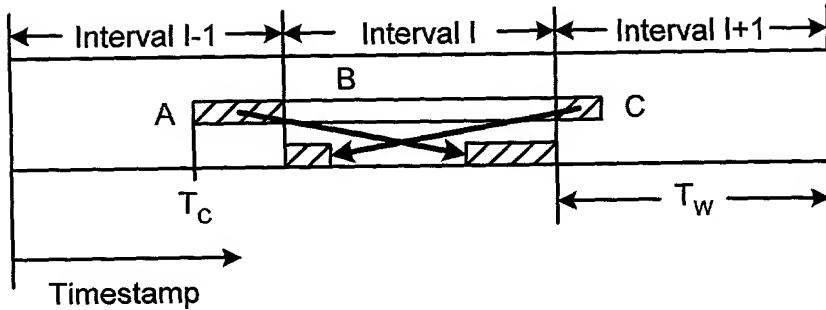


Fig. 6a

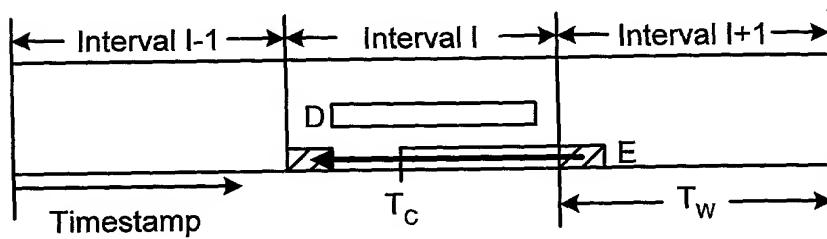


Fig. 6b

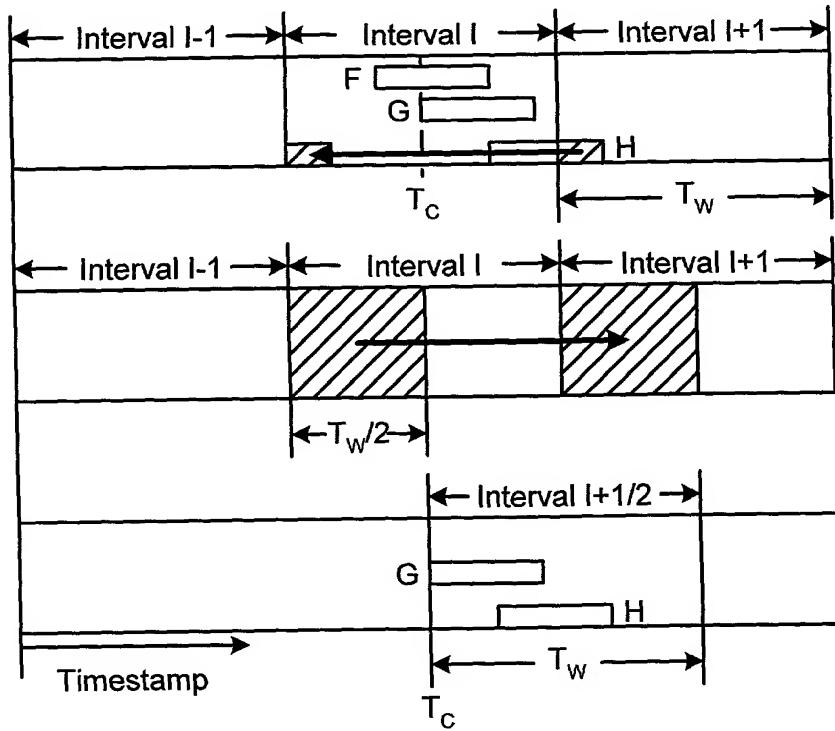


Fig. 6c

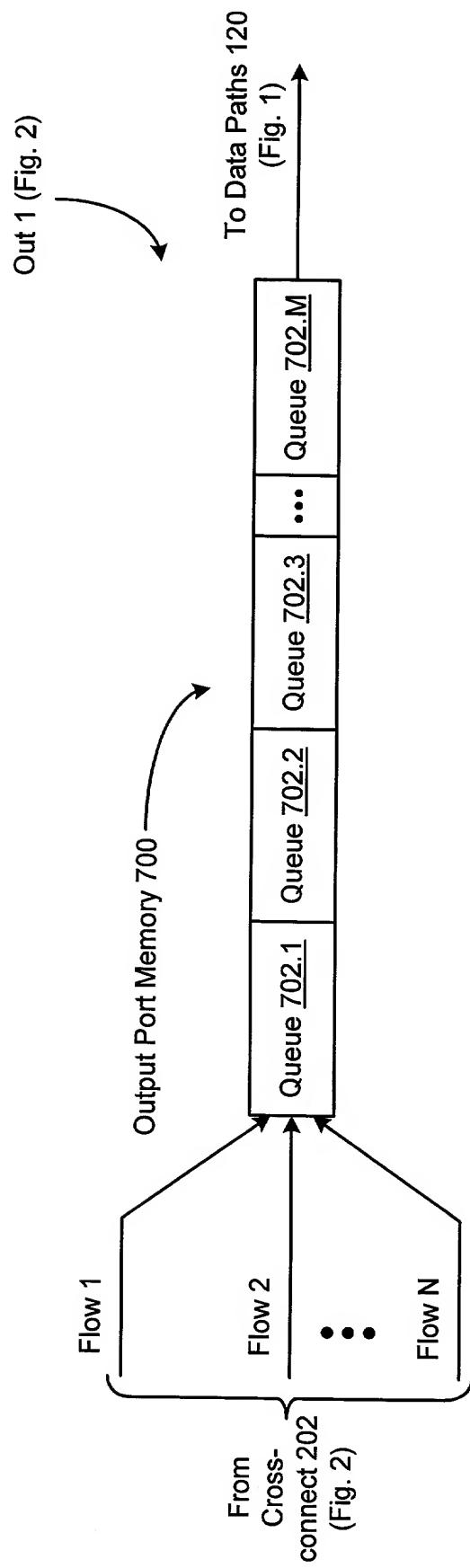


Fig. 7

//RAM1 = First Level Acceleration Bit-string Memory
//RAM2 = Second Level Acceleration Bit-string Memory
//RAM3 = Third Level Acceleration Bit-string Memory
//ARRAY = Linear Time-Indexed Array
//T = Timestamp Value
//T = T1||T2||T3||TA
// where T1 = First Timestamp Value Sub-field
// T2 = Second Timestamp Value Sub-field
// T3 = Third Timestamp Value Sub-field
// TA = Fourth Timestamp Value Sub-field
// P = Packet Descriptor
ARRAY[T] <-- P //Timeslot is marked "Used" (Used=1).
RAM1<T1> <-- 1
RAM2[T1]<T2> <-- 1
RAM3[T1||T2]<T3> <-- 1

Fig. 8

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//x1 = First Level Priority-encoded Acceleration
//Bit-string
//x2 = Second Level Priority-encoded Acceleration
//Bit-string
//x3 = Third Level Priority-encoded Acceleration
//Bit-string
x1 <-- PRI(RAM1)
x2 <-- PRI(RAM2[x1])
x3 <-- PRI(RAM3[x1||x2])
X <-- x1||x2||x3
//Read N entries of ARRAY starting with ARRAY[X].
P <-- ARRAY[K] //K = the index of the first "Used"
 //ARRAY entry read. Timeslot is
 //marked "Unused" (Used=0).
RAM3[x1||x2]<x3> <-- 0 //In the event all ARRAY[X]
 //through ARRAY[X+N-1] are
 //now Unused.
RAM2[x1]<x2> <-- 0 //In the event RAM3[x1||x2] = 0.
RAM1<x1> <-- 0 //In the event RAM2[x1] = 0.

Fig. 9